Weekly status – 3/3/2014

Task – Defining project scope, short term goals, and long term research goals –

Progress – Sent out a brief outline of proposal to Dr. Tessier. There are plenty of open ended aspects in the document but the goal is to get clarity on some of the aspects outlined in the proposal as we go forward with the research.

Blocking issues - None

Task – Getting started with setting up environment, research tools etc.

Progress- was able to go to the lab and work over the weekend. I now have the software environment and tool setup necessary to do some synthesis work. Have downloaded and started playing around with Altera Quartus tools. Studied some aspects of the DE4 board.

Blocking issues – I currently have a 30 day limited license to use the tools. Apparently, the team has access to tools as well as floating licenses for running these tools. I might need some help either with assigning me a machine in the lab through which I can vnc in remotely to do my work, or permission to being my own machine and set it up in the lab so I can work remotely and use the tools necessary for research. Need access permission from Dr. Tessier

Task – Study the research on switchbox architecture and see how to integrate it into existing work for supporting course grained reconfigurability

Progress – One of the things identified as part of the initial tasks was to work on switchbox architecture to support Xiaomin’s research effort. This week, I spent time on reading up on switchbox architectures by various groups and how it was done in context of reconfigurable architectures. After spending time on background research, I went on to start outlining a document describing the pros/cons of various approaches. The document is not yet complete for review. Also, I did some research on obtaining a template of switchbox Verilog code which we can obtain as starting point. There is an opensource that Stanford University NOC group has put out that can be used as starting point. I have to prune it substantially to get it into a usable format for our purposes (as we need something much lighter and more agile to support dynamic reconfigurability). Next week I will start pruning this RTL to structure that we might be interested in. In addition, we need to start looking into how this switchbox will interact with processors/memory. So interface definition is something we will need to look into soon, probably next week.

Blocking issues - None

Task – Study the NIOS/Spree architectures

Spent some time reading up on NIOS processors that are provided as part of the Altera toolset. Seems fairly standard. The programming etc. also seems fairly straightforward just like any device driver activity. I have not yet done any real synthesis/simulation work on this but plan on doing that next week.

One of the suggestions as part of the research was that at later stages, we will like to replace NIOS cpu’s with open source SPREE cores. So downloaded the tool and started building some base level cores as outlined in their manual. It was fairly straightforward. Will try and start some basic synthesis work on these cores and see if I can get a simulation model up and running with some benchmarks. Hope to make some progress on this next week.

Blocking issues – None

Task – Start looking into StreamIT compiler for studying how to build compiler for course grained reconfigurable architectures

Progress – downloaded StreamIT compiler. Started playing around with it wrt making the toolset etc. have to start running benchmarks on it and studying the data. Have started reading the research background. Currently reading Dr. Micheal Gordon’s PhD thesis on StreamIT compiler.

Blocking issues- None

Miscellaneous -

Met the research team and interacted with them

Discussed technical aspects of research with Xiaobin

Exchanged emails with Professor in defining project goals more clearly. There is work needs to be done but my goal is to update this document biweekly and send it to Professor based upon progress.